REMARKS

This is intended as a full and complete response to the Final Office Action dated November 13, 2006, having a shortened statutory period for response set to expire on February 13, 2007. Applicant submits this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-4, 6-15 and 17-18 are pending in the application. Claims 1-4, 6-15, 17-18 and 22-24 remain pending following entry of this response. Claims 7 and 11-12 have been amended. Claims 5, 16 and 19-21 have been canceled. New claims 22-24 have been added to recite aspects of the invention. Applicant submits that the amendments and new claims do not introduce new matter.

Claim Rejections - 35 U.S.C. § 112

Claims 12-15 & 17 are rejected under 35 U.S.C. 112, second paragraph. The claims have been amended to remove reference to a second switching device. Accordingly, Applicant respectfully requests withdrawal of this rejection.

Claim Rejections - 35 U.S.C. § 102

Claims 1-2, 6, and 11 are rejected under 35 U.S.C. 102(e) as being fully anticipated by *Taylor et al.* (U.S. Pat. No. 6,971,051, hereinafter, "*Taylor*"). Applicant respectfully traverses this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

As argued in the previous response to the Office Action mailed May 2, 2006, Applicant respectfully submits that *Taylor* fails to disclose that *control signals from outside of the multi-chip memory module are disconnected during a self-test.*, as claimed in independent claims 1, 12 and 18. As described in paragraphs [0028]-[0030], disconnecting the control signals in this manner allows a common set of terminals of a DRAM, on which the self-test control device is located, to be utilized presented to the outside, while still preventing access from the outside during the self-test.

Applicant further submits that *Taylor* fails to teach a self-test control device located within a DRAM memory chip, at all. In responding to Applicant's argument, the Examiner cites to the following portion of *Taylor*:

> The self-tester capability includes stored test code that is specific to detecting errors within ***the information (e.g., executable code) residing within the volatile memory***. The stored test code includes instructions which implement memory testing routines. ***The test code may be stored within embedded non-volatile memory of the integrated circuit***. [Emphasis Added]

The Examiner concludes that "Here, clearly *Taylor et al.* teaches that the self-test capabilities are located within the volatile memory."

Applicant submits, however, that the Examiner has misconstrued the teachings of *Taylor* and that the above-referenced portion states that the self-tester capability is not located within volatile memory, but rather includes executable code *stored in non-volatile memory* used to detect errors *within information residing within the volatile memory*. In other words, it is the information to be tested that is located in the volatile memory, not the self-tester capability. The test code (i.e., the code that performs the test of the information to be tested), on the other hand, is embedded in non-volatile memory.

This proper construction is further supported in FIG. 3, which clearly shows TEST CODE ROM 68 that is separate from DRAM 56. Further, the corresponding description (col. 5, lines 53-58) clarifies that operation of the self-test capability involves interaction of a processor that executes the self test code contained in TEST CODE ROM 68:

> However, the ASIC does include non-volatile read only memory (ROM) 68 that stores the test code which is used by the processor 58 in performing the self-testing. As a consequence of having the stored test code, printer firmware is able to perform volatile memory checking periodically when the system is inactive (col. 5, lines 53-58)

Thus, the self-test capability taught by *Taylor* clearly is not contained in a DRAM and, further, involves processor interaction. This is in stark contrast to the self-test capability claimed in the present application that is located within a DRAM device and relieves a processor from most of the overhead conventionally associated with self-test operations (as described in paragraph [0045]).

For these reasons, Applicant submits that independent claims 1, 12 and 18, as well as their dependents are allowable and respectfully request withdrawal of this rejection.

Claim 11 has been re-written in independent form to include the limitations of claim 1 and is, therefore, allowable for the reasons given above with respect to claim 1. Further, Applicant would like to separately address statements made by the Examiner. In rejecting previous claim 11 (in dependent form), the Examiner cited column 5, lines 3-21 of *Taylor* as teaching performing self-tests during or after battery charging of an application apparatus. Applicant respectfully submits, however, that *Taylor* makes no mention of charging a battery at all, and certainly no mention of performing self-test operations during a re-charge. As described in the present application, battery charging presents a convenient time for the claimed self-test operations as times when DRAM under test is not being accessed.

For these reasons, Applicant submits that independent claim 11, as well as its dependents are also allowable and respectfully request withdrawal of this rejection with respect to these claims.

Claim Rejections - 35 U.S.C. § 103

Claims 3-4 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Taylor*, and further in view of *Barr* (U.S. Pat. No. 5,758,056). Claims 12-15, 17 and

18 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Taylor*, and further in view of *Barr* and previously cited *Lai*. Applicant respectfully traverses this rejection.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143.

Regarding claims 3-4, 7-10, Applicant submits that these claims depend from claims 1, which is allowable for reasons discussed above. Accordingly, Applicant submits these claims are also allowable.

Regarding claim 12, Applicant submits that the claimed combination of references fail to teach *a self-test control device, disposed in one of the DRAM memory chip and the nonvolatile memory chip, for conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operating mode of the application apparatus and a switching device for disconnecting the control inputs at the DRAM memory chip and at the nonvolatile memory chip from outside the multichip memory module; and wherein the self-test control device provides signals to control inputs of the DRAM memory chip and control inputs of the nonvolatile memory chip*, as recited in the claim. In other words, even in combination, *Barr* and *Lai* fail to overcome the deficiencies of the teachings of *Taylor*. Thus, Applicant submits claim 12 and its dependents are allowable.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

If the Examiner believes any issues remain that prevent this application from going to issue, the Examiner is strongly encouraged to contact the undersigned attorney to discuss strategies for moving prosecution forward toward allowance.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

/Gero G. McClellan, Reg. No. 44,227/
Gero G. McClellan
Registration No. 44,227
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicant